Davide Zoni

Date of birth	-
Citizenship	Italian
Current position	Assistant Professor (with tenure) - RTDB
Affiliation	DEIB - Politecnico di Milano /
	DIA - Universitá degli Studi di Parma
Address	Campus Bassini - Building 21 - 20133 Milano, Italy
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HIGHLIGHTS

I. **Scientific production, academic qualifications, awards, chairing and editorial service:**

- National (Italian) Scientific Qualification for the role of Associate Professor **Abilitazione Scientifica Nazionale (ASN)**, 2018-2020 Bando D.D. 2175/2018, Settore Concorsuale: 09/H1 Sistemi di Elaborazione delle Informazioni, Fascia: II (period of validity: July 30 2020 - July 30, 2029 - art.16, comma 1, Legge 240/2010)
- Ph.D. in Information Technology at Politecnico di Milano (cum laude) on March 21, 2014
- **21 international journal papers (16 in 1^{st} and 2^{nd} class according to the ANVUR ranking)**, 30 refereed international conference and workshop papers, 1 book chapter, 1 keynote, 1 tutorial, 5 invited talks, and 2 patents
- 2 European Projects (EP) with leading roles: **Task leader** (H2020 FET-HPC MANGO), **Work Package Leader** (FP7-ICT HARPA). 4 other European Projects with research team member role
- **Handling Editor of the Elsevier MICPRO journal**. Program co-chair of AISTECS 2019 workshop (co-located with HiPEAC) and Guest Editor for the Journal of Low Power Electronics and Applications (JLPEA) in 2019
- Technical Program Committee (TPC) member of the Design, Automation and Test in Europe (DATE), ACM/IEEE International Symposium on Low Power Electronics and Design (ISLPED), Euromicro Conference on Digital System Design (DSD) and IEEE ReCoSoC. TPC member of CS2 and PARMA-DITAM workshops (co-located with HiPEAC)
- Winner of the *Switch2Product (S2P) - Innovation Challenge* in 2019 [1]
- **Principal investigator** of 6 developed tools/intellectual properties (IPs) that have been/are actively used within the HEAPLab[2] research group to support master and PhD students as well as the technology trasfer activities of the candidate. In general, the design and development of the tools have been partially funded by the European Commission or private Venture Capitalists (see Section Tools and intellectual properties (IPs): design and implementation).
- Member of IEEE

II. **Teaching experience in the last three academic years:**

- 2020-21 / 2021-22: Fondamenti di Informatica (60 hours - 6 CFU, **Lecturer**) - B.Sc.-IT, Ingegneria Edile e delle Costruzioni, Politecnico di Milano
- 2019-20 / 2020-21 / 2021-22: Embedded systems (48 hours - 6 CFU, **Lecturer**) - M.Sc.-IT, Computer Science and Engineering, Universitá degli Studi di Parma

[1] https://s2p.it
[2] http://heaplab.deib.polimi.it/

- 2020-2021: Verilog, SystemVerilog e VHDL avanzati - Systematic and object-oriented functional verification in SystemVerilog (40 hours - **Lectuter**) - Industrial course, Cefriel srl, Italy.
- 2020-2021: Designing modern processors: a perspective on power consumption, security, reliability, and efficient programming (25 hours - 5 CFU **Lectuter**) - PhD/MSc course, Computer science and engineering, University of Zaragoza, Spain.
- 2020-21: Digital Design of Embedded Systems in the IoT and RISC-V open core era (25 hours - 5 CFU, **Lecturer**) - PhD course - Politecnico di Milano, PhD Program in Information Technology
- 2019-20: Digital Design of Embedded Systems (DDES) (24 hours - 4 CFU, **Lecturer**) - PhD course - Universitá degli Studi di Parma, PhD Program in Information Technology
- 2019-20 / 2020-21 / 2021-22: Architetture dei Calcolatori e Sistemi Operativi (ACSO) (40 hours, **Teaching Assistant**) - B.Sc.-IT, Ingegneria informatica, Politecnico di Milano
- 2019-20 / 2020-21 / 2021-22: Embedded Systems 1 (20 hours, **Teaching Assistant**), M.Sc.-EN, Computer Science and Engineering, Politecnico di Milano

III. **Technology transfer:**

- Founder and CEO of the *Blue Signals Srl* that is a start-up and an **accreditated spin-off** of the Politecnico di Milano targeting hardware design and security. The start-up is innovative (*innovativa* according to the Italian law) and takes steps from the Lightweight Application-Specific Modular Processor (LAMP) research project.
- **Principal investigator** of the LAMP Proof-of-Concept (POC) project.
  Professional investor: 360 Capital Partners[3] via the Poli360 fund ($>$ 150,000€)
- **Two patents** (italian patent + PCT for each technology) related to the industrial development of the LAMP POC project
- Participation to the PoliHUB start-up acceleration program and menthorship (Dec 2019 - June 2020)
- 3 grants to support research activities all of them with the role of **principal investigator/project owner** (a cumulative of 51,000€); *i) OPRECOMP* grant (6,000€), *ii) Eurolab4HPC - Business Prototyping Projects in HPC* (15,000€) and *iii)* the S2P-2019 grant from e-Novia Spa (30,000€)
- 4 European Community grants to support visiting activities of young research fellows (a cumulative scholarship of 22,000€). Two HiPEAC collaboration grants in 2013 and 2014 and two HiPEAC Industrial grants in 2015 and 2017

IV. **Other titles:**

- "Abilitazione alla Professione di Ingegnere
  Settore dell'Informazione, Sezione A, anno 2019, seconda sessione" (79/100)

[3] http://www.360cap.vc/

Contents

1 Position and Education

RECORD OF EMPLOYMENT

June 1, 2021 – now

Assistant professor with tenure - (RTDB - Italian law n.240/2010)

Contract professor at the Dipartimento di Architettura e Ingegneria, Universitá degli Studi di Parma.

February 28, 2020 - May 31, 2021

Contract professor at the Dipartimento di Elettronica Informazione e Bioingegneria (DEIB), Politecnico di Milano.

Contract professor at the Dipartimento di Architettura e Ingegneria, Universitá degli Studi di Parma.

Novembre 11, 2019 - Novembre 10, 2020 (Collaboratore esterno)

Title: "Stima e controllo a livello microarchitetturale del consumo energetico di sistemi embedded"

Research manager: Prof. W. Fornaciari (william.fornaciari@polimi.it)

University: DEIB, Politecnico di Milano.

SSD: Ing-Inf/05, Area: 09

September 1, 2018 - October 31, 2019 (Collaboratore esterno)

Title: "Modellazione a livello micro-architetturale del consumo di potenza"

Research manager: Prof. W. Fornaciari (william.fornaciari@polimi.it)

University: DEIB, Politecnico di Milano.

SSD: Ing-Inf/05, Area: 09

September 1, 2015 - August 31, 2018 (Assegnista di ricerca - Italian law n.240/2010 - art.22)

Title: "Progettazione di architetture di calcolo multi/many-core, con comunicazione basata su NoC, con l'obiettivo di migliorare affidabilita e gestione run-time delle risorse di calcolo"

Research manager: Prof. W. Fornaciari (william.fornaciari@polimi.it)

University: DEIB, Politecnico di Milano.

SSD: Ing-Inf/05, Area: 09

April 16, 2014 - August 31, 2015 (Assegnista di ricerca - Italian law n.240/2010 - art.22)

Title: "Calcolo many-core progettazione di architetture di calcolo multi-core, con sistema di comunicazione basato su noc, con particolare riferimento alla affidabilita e alla gestione run-time delle risorse di calcolo"

Research manager: Prof. W. Fornaciari (william.fornaciari@polimi.it)

University: DEIB, Politecnico di Milano.

SSD: Ing-Inf/05, Area: 09

April 1, 2013 - March 31, 2014 (Assegnista di ricerca - Italian law n.240/2010 - art.22)

Title: "Tecniche di modellizzazione, simulazione e ottimizzazione di fenomeni termici e di invecchiamento in sistemi di calcolo many-core"

Research manager/advisor: Prof. W. Fornaciari (william.fornaciari@polimi.it)

University: DEIB, Politecnico di Milano.

SSD: Ing-Inf/05, Area: 09

April 1, 2011 - March 31, 2013 (Assegnista di ricerca)

Title: "Tecniche di ottimizzazione power-performance per sistemi multicore eterogenei"

Research manager/advisor: Prof. W. Fornaciari (william.fornaciari@polimi.it)

University: DEI, Politecnico di Milano.

SSD: Ing-Inf/05, Area: 09

Jannuary 1, 2011 - March 21, 2014 (PhD Student in Information Technology)

Title: "Exploring power reliability and performance aspects in on-chip networks for multi-cores"

Advisor advisor: Prof. W. Fornaciari (william.fornaciari@polimi.it)

University: DEIB, Politecnico di Milano.

SSD: Ing-Inf/05, Area: 09

EDUCATION

- Ph.D. in Information Technology at Politecnico di Milano (cum laude) on March 21, 2014.
  Title: *"Exploring power reliability and performance aspects in on-chip networks for multi-cores"*
  Advisor: Prof. *W. Fornaciari*
  Reviewers: Prof. *C. Brandolese*, Prof. *F. Catthoor* (IMEC, Belgium), Prof. *J. Flich* (UPV, Spain), Prof. *D. Soudris* (ICCS, Greece)

  Minor Research: *"Server consolidation of multi-tier workloads including performance and reliability constraints"* (March 2011 - November 2011).
  Advisor: Prof. *P. Cremonesi*
  University: Politecnico di Milano

- M.Sc. in Computer Science Engineering (cum laude) on December 21, 2010.
  Thesis title: *"Gestione Dinamica delle Risorse per Sistemi Embedded Multi-Core e Workload Eterogenei"*
  Advisor: Prof. *W. Fornaciari*
  Reviewer: Prof. *G. Palermo*
  University: Politecnico di Milano

OTHERS

- National (Italian) Scientific Qualification for the role of Associate Professor
  Abilitazione Scientifica Nazionale (ASN), 2018-2020 Bando D.D. 2175/2018, Settore Concorsuale: 09/H1 Sistemi di Elaborazione delle Informazioni, Fascia: II (period of validity: July 30 2020 - July 30, 2029 - art.16, comma 1, Legge 240/2010)

- Esame di Stato - Settore dell'Informazione, Sezione A, anno 2019, II sessione (79/100)

VISITING RESEARCH EXPERIENCES

- Visiting researcher at ARM Ltd, Cambridge, UK (August 2015 - December 2015)

- Visiting researcher at the University of Cyprus, Nicosia, Cyprus (January 2015 - April 2015)

- Visiting researcher at Polytechnic University of Valencia, Valencia, Spain (June 2014 - July 2014)

- Visiting researcher at Polytechnic University of Valencia, Valencia, Spain (June 2013 - Jannuary 2014)

External courses

- *PoliHUB accelerator program*: Start-up acceleration program and menthorship reserved to the winners of Switch2Product-2019 (Dec, 2019 - May 2020)
- *EUROPRACTICE course*: Comprehensive Digital IC Implementation & Sign-Off (Using Cadence tools), STFC Rutherford Appleton Laboratory, UK (Jan 22-26, 2018)
- *EUROPRACTICE course*: Essential Verification with SystemVerilog and UVM, IMEC, Leuven, Belgium (Jan 9-13, 2017)
- *EUROPRACTICE course*: Advanced Synthesis with Encounter RTL Compiler - Online Course (2017)
- *EUROPRACTICE course*: Encounter RTL Compiler - Online Course (2017)
- *EUROPRACTICE course*: SystemVerilog for Design and Verification - Online Course (2016)
- *HiPEAC summer school*: Ninth International Summer School on Advanced Computer Architecture and Compilation for High-Performance and Embedded Systems (ACACES), Fiuggi, Italy, July 14-20, 2013
- *HiPEAC summer school*: Eight International Summer School on Advanced Computer Architecture and Compilation for High-Performance and Embedded Systems (ACACES), Fiuggi, Italy, July 8-14, 2012

Industrial Investment & Technology Transfer

TT.3. Accreditated spin-off of the Politecnico di Milano related to the LAMP project (role: founder)

TT.2. Two patents (pending) filed with TTO, Politecnico di Milano (role: owner)

TT.1. Proof-of-Concept (POC) investment by Poli360 (>150,000€) (role: principal investigator)

Awards

AW.3. Winner of the HiPEAC Tech Transfer Award 2021 - *InspectStudio: security analysis and semi-automatic countermeasures at hardware level against side-channel attacks*

AW.2. Winner of the *Switch2Product 2019 - Innovation Challenge* competition (https://s2p.it). Team leader: D. Zoni - Team advisor: W. Fornaciari - Team members: Andrea Galimberti and Giovanni Scotti.

AW.1. IEEE International Symposium on System-on-Chip (SoC) 2012 Best Paper Award
(IEEE SoC has been merged into IEEE NorCAS in 2015)
D. Zoni, S. Corbetta and W. Fornaciari, "Thermal-Performance Trade-off in Network-On-Chip Architectures", in IEEE International Symposium on System-on-Chip, Tampere, Finland October 11-12, 2012. [doi: http://dx.doi.org/10.1109/ISSoC.2012.6376363].

Grants

GR.8. Switch2Product - Corporate Grant by e-Novia Spa (2019)
"S2P 2019 - Innovation Challenge",
https://s2p.it/ - https://e-novia.it

GR.7. H2020 Eurolab4HPC - Business Prototyping Projects (2019)
"GreenHLS: Green High-Level-Synthesis",
https://www.eurolab4hpc.eu/

GR.6. H2020 OPRECOMP summer of code (2019)
"Design and implement a Floating Point Unit for IoT platforms in Systemverilog",
http://oprecomp.eu/

GR.5. HiPEAC industrial grant (2017)
"Analytical Vulnerability Factor Correlation Study",
Supervisor: Dr. R. Jeyapaul (ARM Ltd)

GR.4. HiPEAC industrial grant (2015)
"Impact of weak memory models on application scalability and hardware design",
Supervisor: Dr. S. Diestelhorst (ARM Ltd)

GR.3. HiPEAC collaboration grant (2014)
"Exploring NoC resynchronization schemes to support DVFS- and NTC-based optimizations",
Supervisors: Prof. Y. Sazeides and Prof. C. Nicopoulos (Univeristy of Cyprus)

GR.2. HiPEAC collaboration grant (2013)
"Dynamic router model and control to optimize power-performance tradeoff in NoCs",
Supervisor: Prof. J. Flich (Polytechnic University of Valencia)

GR.1. IEEE SoCC Travel Grant Award (2012)
D. Zoni and W. Fornaciari, "A Sensor-less NBTI mitigation methodology for NoC architectures",
SoCC'2012 25th IEEE International System-on-Chip Conference, Niagara Falls, New York, USA,
September 12–14, 2012. [doi: http://dx.doi.org/10.1109/SOCC.2012.6398329].

2 Teaching activity

2022-2023

- Fondamenti di informatica (60 hours - 6 CFU, **Lecturer**) - Politecnico di Milano, Laurea in Ingegneria Edile e delle Costruzioni.
- Programmazione per la gestione delle informazioni negli smart buildings (30 hours - 3 CFU, **Lecturer**) - Politecnico di Milano, Laurea in Ingegneria Edile e delle Costruzioni.
- Embedded systems (48 hours - 6 CFU, **Lecturer**) - Universitá degli Studi di Parma, Laurea specialistica in Ingegneria Informatica.
- Architetture dei Calcolatori e Sistemi Operativi (ACSO) (40 hours, Teaching Assistant - esercitatore) - B.Sc.-IT, Ingegneria Informatica, Politecnico di Milano, 1st semester. Lecturer: Prof. L. Breveglieri.
- Embedded Systems 1 (20 hours, Teaching Assistant - esercitatore) - Graduate level - Master of Science in Information Technology, M.Sc.-EN, Politecnico di Milano, 1st semester. Lecturer: Prof. W. Fornaciari.
- Progettazione hardware in Verilog, SystemVerilog e VHDL - Systematic and object-oriented design and functional verification using Verilog, SystemVerilog, and VHDL (60 hours - Cefriel **Lectuter**) - Industrial course, Cefriel srl, Italy.

2021-2022

- Fondamenti di informatica (60 hours - 6 CFU, **Lecturer**) - Politecnico di Milano, Laurea in Ingegneria Edile e delle Costruzioni.
- Embedded systems (48 hours - 6 CFU, **Lecturer**) - Universitá degli Studi di Parma, Laurea specialistica in Ingegneria Informatica.
- Architetture dei Calcolatori e Sistemi Operativi (ACSO) (57 hours, Teaching Assistant - esercitatore) - B.Sc.-IT, Ingegneria Informatica, Politecnico di Milano, 1st semester. Lecturer: Prof. L. Breveglieri.
- Embedded Systems 1 (30 hours, Teaching Assistant - esercitatore) - Graduate level - Master of Science in Information Technology, M.Sc.-EN, Politecnico di Milano, 1st semester. Lecturer: Prof. W. Fornaciari.
- Passion in action - Programmazione avanzata in Python: strumenti di analisi visualizzazione ed elaborazione dei dati con integrazione a strumenti BIM e CAD (30 hours - 3 CFU), **Lecturer**) - Politecnico di Milano, Laurea in Ingegneria Edile e delle Costruzioni.

2020-2021

- Verilog, SystemVerilog e VHDL avanzati - Systematic and object-oriented functional verification in SystemVerilog (40 hours - Cefriel **Lectuter**) - Industrial course, Cefriel srl, Italy.
- Designing modern processors: a perspective on power consumption, security, reliability, and efficient programming (25 hours - 5 CFU, **Lecturer - for 10 hours**) - PhD/MSc course, computer science and engineering - University of Zaragoza, Spain.
- Digital Design of Embedded Systems in the IoT and RISC-V open core era (25 hours - 5 CFU, **Lecturer - for 15 hours**) - PhD course - Politecnico di Milano, PhD Program in Information Technology.
- Fondamenti di informatica (60 hours - 6 CFU, **Lecturer**) - Politecnico di Milano, Laurea in Ingegneria Edile e delle Costruzioni.

- Embedded systems (48 hours - 6 CFU, **Lecturer**) - Universitá degli Studi di Parma, Laurea specialistica in Ingegneria Informatica.
- Architetture dei Calcolatori e Sistemi Operativi (ACSO) (57 hours, Teaching Assistant - esercitatore) - B.Sc.-IT, Ingegneria Informatica, Politecnico di Milano, 1st semester. Lecturer: Prof. L. Breveglieri.
- Embedded Systems 1 (34 hours, Teaching Assistant - esercitatore) - Graduate level - Master of Science in Information Technology, M.Sc.-EN, Politecnico di Milano, 1st semester. Lecturer: Prof. W. Fornaciari.

2019-2020

- Embedded systems (48 hours - 6 CFU, **Lecturer**) - Universitá degli Studi di Parma, Laurea specialistica in Ingegneria Informatica.
- Digital Design of Embedded Systems (DDES) (24 hours - 4 CFU, **Lecturer**) - PhD course - Universitá degli Studi di Parma, Dottorato di Ricerca in Tecnologie dell'Informazione.
- Architetture dei Calcolatori e Sistemi Operativi (ACSO) (40 hours, Teaching Assistant - esercitatore) - B.Sc.-IT, Ingegneria Informatica, Politecnico di Milano, 1st semester. Lecturer: Prof. L. Breveglieri.
- Embedded Systems 1 (20 hours, Teaching Assistant - esercitatore) - Graduate level - Master of Science in Information Technology, M.Sc.-EN, Politecnico di Milano, 1st semester. Lecturer: Prof. W. Fornaciari.

2018-2019

- Architetture dei Calcolatori e Sistemi Operativi (ACSO) (40 hours, Teaching Assistant - esercitatore) - B.Sc.-IT, Ingegneria Informatica, Politecnico di Milano, 1st semester. Lecturer: Prof. L. Breveglieri.
- Progetto Finale di Reti Logiche (20 hours, Tutor) - B.Sc.-IT, Ingegneria Informatica, Politecnico di Milano, 1st semester. Lecturer: Prof. W. Fornaciari.
- Embedded Systems 1 (20 hours, Teaching Assistant - esercitatore) - Graduate level - Master of Science in Information Technology, M.Sc.-EN, Politecnico di Milano, 1st semester. Lecturer: Prof. W. Fornaciari.

2017-2018

- Architetture dei Calcolatori e Sistemi Operativi (ACSO) (20 hours, Teaching Assistant - esercitatore) - B.Sc.-IT, Ingegneria Informatica, Politecnico di Milano, 1st semester. Lecturer: Prof. L. Breveglieri.
- Progetto Finale di Reti Logiche (20 hours, Tutor) [4] - B.Sc.-IT, Ingegneria Informatica, Politecnico di Milano, 1st semester. Lecturer: Prof. W. Fornaciari
- Embedded Systems 1 (20 hours, Teaching Assistant - esercitatore) - Graduate level - Master of Science in Information Technology, M.Sc.-EN, Politecnico di Milano, 1st semester. Lecturer: Prof. W. Fornaciari.

2016-2017

- Embedded Systems 1 (20 hours, Teaching Assistant - esercitatore) - Graduate level - Master of Science in Information Technology, M.Sc.-EN, Politecnico di Milano, 1st semester. Lecturer: Prof. W. Fornaciari.

2015-2016

- Energy Aware Design of Computing Systems and Applications (24 hours - **Lecturer for 4 hours**) - PhD Course in Information Technology, Department of Electronics, Information and Bioengineering (DEIB), Politecnico di Milano.

[4] I developed the verification/validation environment for VHDL/Verilog using the Xilinx toolchain. Such environment has been used to automatically validate all projects during AA2017/2018. (Sources available at https://gitlab.com/davide.zoni/verificatore_prova_finale_reti_logiche_bsc_polimi)

- Embedded Systems 1 (20 hours, Teaching Assistant - esercitatore) - Graduate level - Master of Science in Information Technology, M.Sc.-EN, Politecnico di Milano, 1st semester. Lecturer: Prof. W. Fornaciari.

2014-2015

- Embedded Systems 1 (20 hours, Teaching Assistant - esercitatore) - Graduate level - Master of Science in Information Technology, M.Sc.-IT, Politecnico di Milano, 1st semester. Lecturer: Prof. W. Fornaciari.

2013-2014

- Embedded Systems 1 (20 hours, Teaching Assistant - esercitatore) - Graduate level - Master of Science in Information Technology, M.Sc.-IT, Politecnico di Milano, 1st semester. Lecturer: Prof. W. Fornaciari.

2012-2013

- Embedded Systems 1 (20 hours, Teaching Assistant - esercitatore) - Graduate level - Master of Science in Information Technology, M.Sc.-IT, Politecnico di Milano, 1st semester. Lecturer: Prof. W. Fornaciari.

3 Supervised Students

Current Ph.D. Students Supervision/Co-Advisor

2. *Andrea Galimberti*, Expected Graduation 2022, "Design of efficient computing platforms for the IoT".
   Ph.D. in Information Technology, Dipartimento di Elettronica, Informazione e Bioingegneria (DEIB), Politecnico di Milano, Milano, Italy.
   Advisor: Prof. William Fornaciari. Co-advisor: Dr. Davide Zoni.

1. *Luca Cremona*, Expected Graduation 2021, "Power modeling and actuation of embedded multi-cores".
   Ph.D. in Information Technology, Dipartimento di Elettronica, Informazione e Bioingegneria (DEIB), Politecnico di Milano, Milano, Italy.
   Advisor: Prof. William Fornaciari. Co-advisor: Dr. Davide Zoni.

M.Sc. Students Supervisor/Co-Advisor

16. *Giuseppe Diceglie*, December 2021, "On the use of Dynamic Frequency Scaling actuator to face side-channel attacks".
    Master of Science in Engineering of Computing Systems, M.Sc., Politecnico di Milano, Milano, Italy.
    Advisor: Prof. Davide Zoni.

15. *Gabriele Montanaro*, December 2021, "Efficient and flexible FPGA design of code-based post-quantum cryptosystem accelerators".
    Master of Science in Engineering of Computing Systems, M.Sc., Politecnico di Milano, Milano, Italy.
    Prof: Dr. Davide Zoni. Co-advisor: Dott. Ing. Andrea Galimberti.

14. *Daniele Parravicini*, December 2020, "Dynamic Frequency Scaling for Artix-7 FPGAs".
    Master of Science in Engineering of Computing Systems, M.Sc., Politecnico di Milano, Milano, Italy.
    Advisor: Prof. William Fornaciari. Co-advisor: Dr. Davide Zoni.

13. *Michele Piccoli*, December 2020, "A methodology to automatically augment the RTL description of generic digital systems".
    Master of Science in Engineering of Computing Systems, M.Sc., Politecnico di Milano, Milano, Italy.
    Advisor: Prof. William Fornaciari. Co-advisor: Dr. Davide Zoni.

12. *Alessio Sacco*, Graduation June 2020, "Side-channel analysis and countermeasure of an embedded system microarchitecture".
    Master in Computer Science and Engineering, M.Sc., Politecnico di Milano, Milano, Italy.
    Advisor: Prof. William Fornaciari. Co-advisor: Dr. Davide Zoni.
    (link: http://hdl.handle.net/10589/164387)

11. *Andrea Galimberti*, July 2019, "Flexible hardware design of the LEDApkc encryption for FPGA".
    Master in Computer Science and Engineering, M.Sc., Politecnico di Milano, Milano, Italy.
    Advisor: Prof. William Fornaciari. Co-advisor: Dr. Davide Zoni.
    (link: http://hdl.handle.net/10589/149397)

10. *Giovanni Scotti*, April 2019, "Exploring microarchitectural design aspects of RISC CPUs in the IoT era".
    Master in Computer Science and Engineering, M.Sc., Politecnico di Milano, Milano, Italy.
    Advisor: Prof. William Fornaciari. Co-advisor: Dr. Davide Zoni.
    (link: http://hdl.handle.net/10589/147415)

9. *Matteo Brevi*, December 2018, "An FPGA design methodology to measure the information side-channel leakage".

Master in Computer Science and Engineering, M.Sc., Politecnico di Milano, Milano, Italy.
Advisor: Prof. William Fornaciari. Co-advisor: Dr. Davide Zoni.
(link: http://hdl.handle.net/10589/144686)

8. *Tamer Ahmed Elatras*, April 2018, "A Flow Control Mechanism for Fully Adaptive Routing Algorithms in On-Chip Networks".
   Master in Electronics Engineering, M.Sc., Politecnico di Torino, Turin, Italy.
   Advisor: prof. Guido masera, Prof. William Fornaciari. Co-advisor: Dr. Davide Zoni.
   (link: https://webthesis.biblio.polito.it/7544/1/tesi.pdf)

7. *Luca Cremona*, December 2017, "A methodology to augment RTL designs with online power monitoring capability".
   Master in Computer Science and Engineering, M.Sc., Politecnico di Milano, Milano, Italy.
   Advisor: Prof. William Fornaciari. Co-advisor: Dr. Davide Zoni.
   (link: http://hdl.handle.net/10589/137505)

6. *Luca Colombo*, April 2017, "A novel Coherence Protocol for Selectively Power Gating the L2 Banks in Multi-Cores to Optimize the Energy-Performance Trade-Off".
   Master in Computer Science and Engineering, M.Sc., Politecnico di Milano, Milano, Italy.
   Advisor: Prof. William Fornaciari. Co-advisor: Dr. Davide Zoni.
   (link: http://hdl.handle.net/10589/133907)

5. *Fabio Pancot*, December 2016, "Exploring the end-to-end compression to optimize the power-performance tradeoff in NoC-based multicores".
   Master in Computer Science and Engineering, M.Sc., Politecnico di Milano, Milano, Italy.
   Advisor: Prof. William Fornaciari. Co-advisor: Dr. Davide Zoni.
   (link: http://hdl.handle.net/10589/132476)

4. *Mauro Belluschi*, September 2016, "Exploring future DNUCA architectures by bridging the application behaviour and the coherence protocol support".
   Master in Computer Science and Engineering, M.Sc., Politecnico di Milano, Milano, Italy.
   Advisor: Prof. William Fornaciari. Co-advisor: Dr. Davide Zoni.
   (link: http://hdl.handle.net/10589/126685)

3. *Andrea Marchese*, July 2016, "A DVFS-Capable Heterogeneous Network-on-Chip Architecture for Power Constrained Multi-Cores".
   Master in Computer Science and Engineering, M.Sc., Politecnico di Milano, Milano, Italy.
   Advisor: Prof. William Fornaciari. Co-advisor: Dr. Davide Zoni.
   (link: http://hdl.handle.net/10589/123531)

2. *Luca Borghese*, September 2015, "A network interface design for networks-on-chip in heterogeneous NUMA multicores".
   Master in Computer Science and Engineering, M.Sc., Politecnico di Milano, Milano, Italy.
   Advisor: Prof. William Fornaciari. Co-advisor: Dr. Davide Zoni.
   (link: http://hdl.handle.net/10589/111741)

1. *Andrea Canidio*, July 2015, "A Power Gating Methodology to Aggressively Reduce Leakage Power in Networks-on-Chip Buffers".
   Master in Computer Science and Engineering, M.Sc., Politecnico di Milano, Milano, Italy.
   Advisor: Prof. William Fornaciari. Co-advisor: Dr. Davide Zoni.
   (link: http://hdl.handle.net/10589/108869)

CURRENT M. SC. STUDENTS SUPERVISION/CO-ADVISOR

1. *Davide Galli*, Expected Graduation April 2022, "Hardware morphing techniques against side-channel attacks".
   Master of Science in Engineering of Computing Systems, M.Sc., Politecnico di Milano, Milano, Italy.
   Advisor: Prof. Davide Zoni. Co-Advisor: Prof. William Fornaciari.

4 Research Vision and Topics

Research vision - The design of computing platforms represents a key enabling factor to sustain the evolution of Internet-of-Things (IoT) and Edge Computing (EC) services. The big data companies, e.g., Google, Apple, Amazon, Alibaba, Baidu and Microsoft, that are now the most profitable ones in the world (having overtaken energy companies), shifted their business from being service providers to vertical market players also developing their own computing platforms to constantly increase the quality of their services. In this scenario, the recent progress in artificial intelligence is allowing such services, i.e., autonomous driving, speech recognition, augmented reality, and recommendation systems, to move out of from the cyberspace and interact with the real world thus delegating Information and Communication Technology (ICT) platforms to directly control physical and potentially lethal systems, i.e., cars, planes.

Trust represents the key for the social acceptance of such innovative IoT and edge computing services gathering together security, privacy, and safety requirements that emerge side by side with the standing computing efficiency one. However, it has been proven the hardness or even the impossibility of addressing such requirements at the sole software level. In contrast, the hardware level must address all and each of those challenges during the design of the computing platform. For example, computing efficiency is achieved by designing computing platforms tailored to running services and also able to self-adapt depending on the run-time conditions. Moreover, efficient security, especially against the well-known implementation attacks, a.k.a. side-channel attacks, can be solely approached at the hardware level. The current ICT trends highlight a new vision for the hardware researcher which has to account for current software services and their related challenges during the design of efficient and trustful computing system.

As the result of my vision and my experience in designing efficient and secure computing platforms, I proposed the Lightweight Application-specific Modular Processor (LAMP) platform (http://lamp-platform.org). The LAMP-platform initially started as an open-hardware RISC-V-based System-on-Chip specifically tailored for FPGA prototypes although it can be implemented targeting the ASIC technology and it offers three significant advantages with respect to the other open-hardware solutions. First, it is designed to support the research in machine learning and artificial intelligence applications thanks to its easy setup that makes the use of the computing platform extremely easy even for non-hardware researchers. Second, the flexibility of the design allows customizing the final prototype to fit even in small cost-effective FPGAs. Last, it offers a unique set of hardware-level features, i.e., hardware-level online power monitoring and control, hardware security support and Dynamic Frequency Scaling (DFS), to support the research of innovative computing platforms.

By the end of 2019, the LAMP-platform initiative has been supported by three different grants. First, the OPRECOMP Summer of Code grant supported the development of an ultra-low-power and configurable FPU. Such FPU is meant to optimize the computation of Artificial Intelligence tasks in portable devices. Second, the *Eurolab4HPC* grant supported the development of an hardware methodology to automatically implement all-digital power monitors and controllers for general purpose computing platforms. Last, the *Switch2Product* grant by *e-Novia S.p.a.* (30,000€) is supporting the design and the implementation of a general-purpose computing platform that can resist to implementation attacks, i.e., side-channel attacks.

In early 2020, two patents related to the design of a technology to protect general-purpose embedded Systems-on-Chip from side-channel attacks were filed in collaboration with the Technology Transfer Office (Politecnico di Milano). Moreover, the 360 Venture Capital professional investor started supporting the project with a Proof-of-Concept (POC) investment exceeding 150,000€and I took the role of principal investigator. From the academic research standpoint, the LAMP-platform initiative is fueling the work of several master and doctoral students providing a clean and elegant solution to explore the computer architecture research area. My complete vision and ongoing research has been recently presented in a half-day tutorial at HiPEAC [5] in January 2020 [TT1].

[5] HiPEAC is a European network of almost 2,000 world-class computing systems researchers, industry representatives and students. (https://www.hipeac.net/)

Research topics - My research topics are focused on the design methodologies for single- and multi-core embedded platforms at both architectural and microarchitectural abstraction levels. The design of secure and low-power computing platforms to support the innovate services highlighted by the IoT and edge computing paradigm represents a key topic of my investigation. In particular, my research can be seen as organized in two branches that remain tightly connected due to the cross-related knowledge required in each of them: (I) Energy-performance optimization methodologies for multi-cores and (II) Microarchitectural design and verification of secure and low-power architectures for the Internet-of-Things (IoT).

(I) Energy-performance optimization methodologies for multi-cores

With the multi-core revolution, the design architects' focus shifted from the computational logic, i.e., CPUs, to the *uncore*, namely the on-chip interconnect and the cache hierarchy, to sustain the required data communication imposed by the ever increasing number of integrated on-chip CPUs. Moreover, the *uncore* strongly affects the system-wide performance other than being the primary source of the on-chip power consumption. My research in this area focuses on the optimization of the on-chip interconnect in single- and multi-cores also addressing the design of novel cache coherence protocols to support physically distributed, logically shared cache hierarchies. On one hand, I explored the use of standard actuators, e.g., power gating and Dynamic Voltage and Frequency Scaling (DVFS), to design novel energy-performance optimizations NoC architectures [J5, J2]. On the other hand, I presented the design of novel on-chip interconnects [J4] and cache hierarchy architectures [J7]. In particular, the work in [J4] discusses an NoC architecture that can dynamically reallocate the NoC resources to different traffic streams thus optimizing the performance with a net resource decrease also ensuring deadlock fredomness at both protocol- and network-level. The work in [J7] presents a novel cache hierarchy architecture for tiled multi-cores and the related cache coherence protocol to dynamically reshape the size of the LLC by selectively powering-off/on selected LLC banks. It is worth noticing that this part of my research strongly relies on the use of effective cycle accurate simulators that must integrate the architecture and the power model of both the novel proposed computing and actuator elements. This fact imposes a balanced effort between the evaluation of new architectural solutions and the need to customize state-of-the-art research simulators to accurately model the additional components, e.g., DVFS and power gating actuators [J3, J1].

(II) Microarchitectural design and verification of secure and low-power architectures for the IoT

The IoT revolution pushes to the limit the low-power requirement especially for battery powered devices. In such a world of smart, self-adaptive objects it is imperative to offer the possibility of constantly monitoring the power consumption of the computing platform in a cost-effective and low-power manner. In contrast to the power-aware design at architectural level, where lumped power models are used to deliver coarse grained power estimates, the design and implementation of run-time power monitors and controllers represent a critical issue to deliver low-power computing platforms. To this extent and starting from an in-depth understanding of the relationship between the power consumption and the microarchitecture of the computing platform, my research also offers a way to implement accurate and all-digital power monitors for both single- [IC21] and multi-core [J10]. In particular, the research provides the first framework to automatically synthesize all-digital, resource-constrained power monitors for generic computing platforms [J16]. Moreover, the design and implementation of an all-digital control-theoretic scheme for single-[J12] and multi-cores [J14] represents another key contribution of my research. Such control scheme allows to coordinate the concurrent optimization of both power-cap and energy-budget constraints also accounting for the performance requirements. It is worth noticing that the controller allows to dynamically change the performance policy, i.e., the algorithm, without invalidating the Lyapunov stability property.

On a different but related perspective, the power consumption has been highlighted as the primary source of information to setup the so-called side-channel attacks (SCAs) that represent a critical security threat to the Internet-of-Things ecosystem. The side-channel attacks can retrieve the secret key of any software- or

hardware-implemented cryptographic primitive by leveraging the relationship between the computed data and one or more non-functional signals emitted by the computing device, e.g., the power consumption. It is important to note that SCAs are totally different from the traditional cryptoanalysis attacks since the latter try to recover the secret key by exploiting some mathematical lacks in the cryptographic function formulation while the former can succeed even in the presence of a mathematically safe cryptosystem. In particular, SCA countermeasures must consider the microarchitectural implementation of the computing device, thus moving the security evaluation at the hardware level. A complete map of the side-channel leakage sources in an IoT CPU microarchitecture has been presented in [J8] also offering an overview of the link between the architectural and microarchitectural states of the computing platform that is essential to design secure software for general-purpose CPUs. Moreover, a novel solution to design hardware-implemented cryptographic primitives as well as a hardware design flow to promote the security aspect to the role of hardware design metric have been proposed in [J13] and [IC27], respectively.

To provide an effective means to effectively investigate the new challenges of the IoT era, e.g., security, efficiency, machine learning integration in embedded systems, etc, I introduced the Lightweight Application-specific Modular Processor (LAMP) project (`http://lamp-platform.org`) to offer a unique platform for investigating such different research directions. The CPU of the LAMP computing platform has been presented in [J11]. The key goal of the project is to offer a modular, open-hardware platform that can be shaped using, at each time, the minimum number of architectural components to mount the system for the specific investigation as discussed in my research vision that has been presented to the research community in IEEE PDP2019 keynote [KN1] and HIPEAC 2020 tutorial [TT1].

Considering the computational problem of using machine learning applications in the embedded system domain, the LAMP platform is equipped with a novel floating-point unit (FPU) implements a true hardware-software co-design to offer the best-in-class resource-energy-performance trade-off [J17]. Moreover, a new set of benchmarks has been developed to investigate machine learning and computer vision applications executed on bare-metal embedded systems [C28].

Concerning the hardware security research area, the flexibility and modularity of the LAMP platform makes gate-level simulations a viable option since the microarchitecture can stay small. To this end, a complete analysis of the hardware-level security challenges in the IoT general-purpose computing platforms has been discussed in my IEEE ReCoSoC-2019 invited talk [TK5]. Moreover, we have filed two patents in collaboration with the Technology Transfer Office (Politecnico di Milano). The first patent describes a novel technology to accurately synchronize the prototype execution of a computing platform with either the RTL simulation of the same platform or the acquisition of an environmental parameter generated by the same platform [PT1]. The second patent presents a hardware technology to secure general-purpose embedded computing platforms from emission-based side-channel attacks.

Considering the upcoming quantum-computing threat to the security of modern cryptographic primitives, my research is also devoted to the implementation of custom hardware accelerators to efficiently execute the most time-consuming computations in code-based post-quantum cryptographic schemes. In particular, a flexible hardware-implemented binary polynomial multiplier has been proposed to support QC-LDPC post-quantum encoding schemes [J15, C27]. Moreover, a flexible bit-flipping decoder has been proposed to support the decryption of QC-LDPC post-quantum cryptosystems [J18]. To effectively trade performance with resource utilization, the multiplier and the bit-flipping decoder have been designed to scale across the entire family of the Xilinx Artix-7 mid-range FPGAs.

5 Professional Activities

INDUSTRIAL/RESEARCH PROJECTS

- Proof-of-Concept (POC) - Side-channel resistant general-purpose SoC
  Name - Design a side-channel resistant general-purpose computing platform
  Duration (Kick-off)- 15 months (May, 2020)
  Project Owners - Dr. Davide Zoni (Principal inverstigator) and Prof. W. Fornaciari (Scientific advisor)
  Professional investor(s) - 360 Capital Partners[6] via the Poli360 fund ($>$ 150,000€)
  Role - **Principal Investigator**
  Activity - Coordinate and partecipate the technical and strategic activities of the entire project considering *i)* the design of the computing platform and the side-channel countermeasure, *ii)* the design of the side-channel vulnerability assessement framework and *iii)* technical and strategic reporting activity
  Investment amount - $>$ 150k€ (Details are under Non-Disclosure-Agreement (NDA))

EUROPEAN RESEARCH PROJECTS

- H2020-EuroHPC-956831
  Name - TEXTAROSSA: Towards EXtreme scale Technologies and Accelerators for euROhpc hw/Sw Supercomputing Applications for exascale
  Duration (Kick-off)- 36 months (April 1, 2021)
  Project Coordinator - Dr. M. Celino, CINECA, Italy
  Local Project Leader - Prof. William Fornaciari (william.fornaciari@polimi.it)
  Role - **Task Leader (T4.5)**
  Activity - In T4.5 power modeling and control in general purpose computing platforms.

- H2020-FETHPC-801137
  Name - RECIPE: REliable power and time-ConstraInts-aware Predictive management of heterogeneous Exascale systems
  Duration (Kick-off)- 36 months (May 1, 2018)
  Project Coordinator - Prof. W. Fornaciari, Politecnico di Milano, Italy
  Local Project Leader - Prof. William Fornaciari (william.fornaciari@polimi.it)
  Role - Research team member
  Activity - In T4.1 development and adaptation of the power model to cover heterogenous hardware resources. In T4.2 contributed to the integration of the hardware resources with the run-time resource manager.

- H2020-FET-671668
  Name - MANGO: exploring Manycore Architectures for Next-GeneratiOn HPC systems
  Duration (Kick-off)- 42 months (Oct 1, 2015)
  Project Coordinator - Prof. J. Flich, Polythecnic University of Valencia, Spain
  Local Project Leader - Prof. William Fornaciari (william.fornaciari@polimi.it)
  Role - **Task Leader (T2.3), Runtime Resource Management System Support**
  Activity - Design and Implementation the RTL power model to be used at software level for resource management optimizations.

- FP7-ICT-612069
  Name - HARPA: Harnessing Performance Variability
  Duration (Kick-off)- 39 months (Sept 1, 2013)

[6] http://www.360cap.vc/

Project Coordinator - Prof. William Fornaciari, Politecnico di Milano, Italy
Local Project Leader - Prof. William Fornaciari (william.fornaciari@polimi.it)
Role - **Work Package Leader (WP1), HARPA OS**
Activity - Analysis, Design and Implementation of (i) low level monitors and actuators for power-performance-reliability optimizations (ii) optimization policies and required infrastructure to make the estimates and actuation capabilities from hardware level up to the Operating System.

- FP7-ICT-611146
  Name - CONTREX: Design of embedded mixed-criticality CONTRol systems under consideration of EXtra-functional properties
  Duration (Kick-off)- 39 months (Sept 1, 2013)
  Project Coordinator - Dr. Kim Gruttner, OFFIS EV, Germany
  Local Project Leader - Prof. William Fornaciari (william.fornaciari@polimi.it)
  Role - Research team member
  Activity - Contributed to T3.3 focusing on run-time management of resources

- FP7-ICT-248716
  Name - 2PARMA: PARallel PAradigms and Run-time MAnagement techniques for Many-core Architectures
  Duration (Kick-off)- 36 months (Jan, 2010)
  Project Coordinator - Prof. Cristina Silvano, Politecnico di Milano, Italy
  Local Project Leader - Prof. Cristina Silvano (cristina.silvano@polimi.it)
  Role - Research team member
  Activity - Design and implementation of the initial resource management policy, that has been later extended in the Barbeque Open Source Project (http://bosp.dei.polimi.it/).

- FP7-JTI-ARTEMIS-100230
  Name - SMECY: Smart Multicore Embedded systems
  Duration (Kick-off)- 36 months (Feb 1, 2010)
  Project Coordinator - Commissariat a l'energie Atomique (France)
  Local Project Leader - Prof. Donatella Sciuto (donatella.sciuto@polimi.it)
  Role - Research team member
  Activity - Contributed the research on run-time resource management solutions at software-level

SCIENTIFIC COLLABORATIONS BEYOND EU-PROJECTS

- Dep. of Computer Science and Systems Engineering at University of Zaragoza, Spain (2019 - ongoing)
  Contact - prof. Alex Valero (alvabre@unizar.es)
  Research Activity - Reliable and efficient embedded computing platforms

- Robotics and machine learning group at DEIB - Politecnico di Milano, Italy (2019 - ongoing)
  Contact - prof. Matteo Matteucci (matteo.matteucci@polimi.it)
  Research Activity - Moving vision and AI tasks to IoT platforms by means of ad-hoc hardware accelerators

- Cryptography group at DEIB - Politecnico di Milano, Italy (Jul 2015 - ongoing)
  Contacts - prof. Giampaolo Agosta (giovanni.agosta@polimi.it),
  prof. Alessandro Barenghi (alessandro.barenghi@polimi.it),
  prof. Gerardo Pelosi (gerardo.pelosi@polimi.it)
  Research Activity - Hardware Countermeasures to Side-Channel Attacks

- ARM Research - ARM Cambridge, UK (Sept 2015 - 2020)
  Contact - Dr. Stephan.Diestelhorst (Stephan.Diestelhorst@arm.com)
  Research Activity - Coherence protocol and on-chip solutions for big.LITTLE architectures

- *multiCAL* group at University of Cyprus, Cyprus (Jan 2015 - 2019)
  Contacts - prof. Yanos Sazeides (yanos@cs.ucy.cy),
  prof. Chrys Nicopoulos (nicopoulos@ucy.ac.cy)
  Research Activity - Power gating methodologies for reliable and low-power multicores.

- Automation and Control group at DEIB - Politecnico di Milano, Italy (2017 - 2019)
  Contact - prof. Marcello Farina (marcello.farina@polimi.it)
  Research Activity - Distributed control methodologies at RTL level to efficiently support power-performance optimization schemes for embedded systems

Chairing and Editorial Service in Journals, Conferences and Workshops

2021

- Supervising Handling Editor of Elsevier MICPRO Special Issue: Low Power Consumption Embedded Devices in IoT Microsystems
- Handling Editor of Elsevier MICPRO

2020

- Handling Editor of Elsevier MICPRO

2019

- Guest Editor Journal of Low Power Electronics and Applications (JLPEA)
- Program Chair AISTECS 2019 (co-located with HiPEAC 2019)

Program Committee Membership

According to the **GII-GRIN-SCIE** conference ranking[7], the "Design, Automation and Test in Europe" (DATE) conference and the "International Symposium on Low Power Electronics and Design" (ISLPED) conference report a GGS rating of "A" and a GGS Class of "2". According to the **Conference Ranks** conference ranking[8] the "Euromicro Digital System Design" (DSD) conference reports a rank of "B1".

2022

- Technical Program Committee Member of DATE 2022:
  Design, Automation and Test in Europe - Track D8 - Networks-on-Chip

2021

- Technical Program Committee Member of IEEE Int. Green and Sustainable Computing Conference (IGSCC)
- Technical Program Committee Member of DATE 2021:
  Design, Automation and Test in Europe - Track D8 - Networks-on-Chip
- Technical Program Commititee Member of Euromicro Conference on Digital System Design (DSD)
- Technical Program Committee Member of ACM PARMA-DITAM:
  Workshop (co-located with HiPEAC)
- Technical Program Committee Member of ACM/IEEE ISLPED 2021:
  International Symposium on Low Power Electronics and Design - Track 1.3 Logic and Architecture

2020

- Technical Program Committee Member of ACM/IEEE ISLPED 2020:
  International Symposium on Low Power Electronics and Design - Track 1.3 Logic and Architecture
- Technical Program Committee Member of DATE 2020:
  Design, Automation and Test in Europe - Track D7 - Networks-on-Chip
- Technical Program Committee Member of IEEE Int. Green and Sustainable Computing Conference (IGSCC)

[7] http://gii-grin-scie-rating.scie.es/
[8] http://www.conferenceranks.com/#data

- Technical Program Committee Member of ACM PARMA-DITAM:
  Workshop (co-located with HiPEAC)

2019

- Technical Program Committee Member of ACM/IEEE ISLPED 2019:
  International Symposium on Low Power Electronics and Design - Track 1.3 Logic and Architecture
- Technical Program Committee Member of DATE 2019:
  Design, Automation and Test in Europe - Track D7 - Networks-on-Chip
- Technical Program Commitee Member of IEEE ReCoSoC 2019:
  International Workshop on Reconfigurable Communication-Centric Systems-on-Chip (ReCoSoC)
- Technical Program Committee Member of ACM PARMA-DITAM:
  Workshop (co-located with HiPEAC)
- Technical Program Committee Member of CS2:
  Security in Computing Systems (CS2) workshop (co-located with HiPEAC)

2018

- Technical Program Committee Member of DATE 2018:
  Design, Automation and Test in Europe - Track D7 - Networks-on-Chip
- Technical Program Committee Member of ACM PARMA-DITAM:
  workshop (co-located with HiPEAC)
- Technical Program Committee Member of ACM CS2:
  Security in Computing Systems (CS2) workshop (co-located with HiPEAC)

2017

- Technical Program Committee Member of ACM CS2:
  Security in Computing Systems (CS2) workshop (co-located with HiPEAC)

REFEREE SERVICES IN INTERNATIONAL JOURNALS AND TRANSACTIONS

I also serve as reviewer in several international peer-reviewed journals and transactions: IEEE Embedded System Letters (IEEE ESL), Journal of Microprocessors and Microsystems (Elsevier MICPRO), Journal of Systems Architecture (Elsevier JSA), Transactions on Parallel and Distributed Systems (IEEE TPDS), Journals on Parallel and Distributed Computing (Elsevier JPDC), Transactions on Embedded Computing Systems (ACM TECS), Transactions on Computer-Aided Design of Integrated Circuits and Systems (IEEE TCAD), Elsevier VLSI Journal.

6 Complete Publication List and Research Products

The research activity took place in a tightly knit collaboration among the authors, thus each author significantly contributed to the publication. For each publication, the first author represents the leading author unless the alphabetic order is used. In the latter case the contribution is supposed to be equally distributed among the authors.

PUBLICATION LIST

Refereed international journals — IJ (21)
Refereed international conferences and workshops — IC (30)
Refereed international books and book chapters — IB (1)
Patents — PT (2)
Keynotes — KN (1)
Tutorials — TT (1)
Invited talks and seminars — TK (5)
PhD Thesis — TH (1)
Principal investigator in research/teaching/industrial tools — TL (6)

Bibliometry: Google Scholar (All - 2017): Citations 502 - 360, h-index 14 - 12, i10-index 24 - 16
Scopus (All): Citations 300, h-index 11

REFEREED INTERNATIONAL JOURNALS

IJ.21. D. Zoni and A. Galimberti, "Cost-effective fixed-point hardware support for RISC-V embedded systems", *Elsevier Journal of Systems Architecture (JSA)*, 2022.
(DOI: https://doi.org/10.1016/j.sysarc.2022.102476)

IJ.20. A. Galimberti, G. Montanaro, and D. Zoni, "Efficient and scalable FPGA design of GF(2m) inversion for post-quantum cryptosystems", *IEEE Trans. on Computers (IEEE TC)*, 2022.
(DOI: https://doi.org/10.1109/TC.2022.3149422)

IJ.19. D. Zoni, L. Cremona, and W. Fornaciari, "Design of side-channel resistant power monitors", *IEEE Trans. on Computer-Aided Design of Integrated Circuits and Systems (TCAD)*, 2021.
(DOI: https://doi.org/10.1109/TCAD.2021.3088781)

IJ.18. D. Zoni, A. Galimberti and W. Fornaciari, "Efficient and scalable FPGA-oriented design of QC-LDPC bit-flipping decoders for post-quantum cryptography", *IEEE Access*, 2020.
(DOI: https://doi.org/10.1109/ACCESS.2020.3020262)

IJ.17. D. Zoni, A. Galimberti and W. Fornaciari, "An FPU design template to optimize the accuracy-efficiency-area trade-off", *Sustainable Computing: Informatics and Systems (SUSCOM)*, Elsevier, 2020.
(DOI: https://doi.org/10.1016/j.suscom.2020.100450)

IJ.16. L. Cremona, W. Fornaciari, and D. Zoni,"Automatic identification and hardware implementation of a resource-constrained power model for embedded systems", *Sustainable Computing: Informatics and Systems (SUSCOM)*, Elsevier, 2020.
(DOI: https://doi.org/10.1016/j.suscom.2020.100467) (Alphabetic order)

IJ.15. D. Zoni, A. Galimberti and W. Fornaciari, "Flexible and scalable FPGA-oriented design of multipliers for large binary polynomials", *IEEE Access*, 2020.
(DOI: https://doi.org/10.1109/ACCESS.2020.2989423)

IJ.14. D. Zoni, L. Cremona and W. Fornaciari, " All-digital control-theoretic scheme to optimize energy budget and allocation in multi-cores", *IEEE Transactions on Computers (TC)*, 2019.
(DOI: https://doi.org/10.1109/TC.2019.2963859)

IJ.13. A. Barenghi, W. Fornaciari, G. Pelosi and D. Zoni, "Scramble Suit: A Profile Differentiation Countermeasure to Prevent Template Attacks" *IEEE Trans. on Computer-Aided Design of Integrated Circuits and Systems (TCAD)*, 2019

(alphabetic order).
(DOI: https://doi.org/10.1109/TCAD.2019.2926389)

IJ.12. D. Zoni, L. Cremona and W. Fornaciari, "All-digital energy-constrained controller for general-purpose accelerators and CPUs", *IEEE Embedded Systems Letters (ESL)*, 2019.
(DOI: https://doi.org/10.1109/LES.2019.2914136

IJ.11. G. Scotti and D. Zoni, "A Fresh View on the Microarchitectural Design of FPGA-Based RISC CPUs in the IoT Era", *Journal of Low Power Electronics and Applications (JLPEA)*, MDPI, 2019.
(alphabetic order)
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IJ.10. D. Zoni, L. Cremona, A. Cilardo, M. Gargliardi, W. Fornaciari, "PowerTap: All-digital Power Meter Modeling for Run-time Power Monitoring", *Microprocessors and Microsystems (MICPRO)*, Elsevier, 2018.
(DOI: https://doi.org/10.1016/j.micpro.2018.07.007)

IJ.9. J. Flich, G. Agosta, P. Ampletzer, D. Atienza Alonso, C. Brandolese, E. Cappe, A. Cilardo, L. Dragić, A. Dray, A. Duspara, W. Fornaciari, E. Fusella, M. Gagliardi, G. Guillaume, D. Hofman, Y. Hoornenborg, A. Iranfar, M. Kovac, S. Libutti, B. Maitre, J. Martínez, G. Massari, K. Meinds, H. Mlinaric, E. Papastefanakis, T. Picornell, I. Piljic, A. Pupykina, F. Reghenzani, I. Staub, R. Tornero, M. Zanella, M. Zapater, D. Zoni, "Exploring Manycore Architectures for Next-Generation HPC Systems through the MANGO Approach", *Microprocessors and Microsystems (MICPRO)* , Elsevier, 2018.
(DOI: https://doi.org/10.1016/j.micpro.2018.05.011)

IJ.8. D. Zoni, A. Barenghi, G. Pelosi, W. Fornaciari, "A Comprehensive Side Channel Information Leakage Analysis of an In-order RISC CPU Microarchitecture", *ACM Transactions on Design Automation of Electronic Systems (TODAES)*, 2018.
(DOI: https://doi.org/10.1145/3212719)

IJ.7. D. Zoni, L. Colombo, W. Fornaciari, "DarkCache: Energy-performance Optimization of Tiled Multi-cores by Adaptively Power Gating LLC Banks", *ACM Transactions on Architecture and Code Optimization (TACO)* , 2018.
(DOI: https://doi.org/10.1145/3186895)

IJ.6. K. Gruttner, R. Gorgen, S. Schreiner, F. Herrera, P. Penil, J. Medina, E. Villar, G. Palermo, W. Fornaciari, C. Brandolese, D. Gadioli, E. Vitali, D. Zoni, S. Bocchio, L. Ceva, P. Azzoni, M. Poncino, S. Vinco, E. Macii, S. Cusenza, J. Favaro, R. Valencia, I. Sander, K. Rosvall, N. Khalilzad, D. Quaglia, "CONTREX: Design of embedded mixed-criticality CONTRol systems under consideration of EXtra-functional properties", *Microprocessors and Microsystems (MICPRO)*,pp. 39-55, Elsevier, 2017.
(DOI: https://doi.org/10.1016/j.micpro.2017.03.012)

IJ.5. D. Zoni, A. Canidio, W. Fornaciari, Panayiotis Englezakis, Chrysostomos Nicopoulos and Yiannakis Sazeides, "BlackOut: Enabling fine-grained power gating of buffers in Network-on-Chip routers", *Journal of Parallel and Distributed Computing (JPDC)*, Elsevier, 2017.
(DOI: https://doi.org/10.1016/j.jpdc.2017.01.016)

IJ.4. D. Zoni, J. Flich and W. Fornaciari, "CUTBUF: Buffer Management and Router Design for Traffic Mixing in VNET-Based NoCs", *IEEE Transactions on Parallel and Distributed Systems (TPDS)*, 2016.
(DOI: https://doi.org/10.1109/TPDS.2015.2468716)

IJ.3. D. Zoni, F. Terraneo and W. Fornaciari, "A DVFS Cycle Accurate Simulation Framework with Asynchronous NoC Design for Power-Performance Optimizations", *Journal of Signal Processing Systems (JSPS)*, Springer, 2016.
(DOI: https://doi.org/10.1007/s11265-015-0989-1)

IJ.2. D. Zoni, F. Terraneo and W. Fornaciari, "A control-based methodology for power-performance optimization in NoCs exploiting DVFS", *Journal of Systems Architecture (JSA)*, Elsevier, 2015.
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(DOI: https://doi.org/10.1109/dsd.2017.51)

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Porto, 2015, pp. 351-354, 2015.
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IC.13. M. Farina, D. Zoni, W. Fornaciari, "A control-inspired iterative algorithm for memory management in NUMA multi-cores", *IFAC*, Proceedings Volumes Volume 47, Issue 3, 2014, pp 6117-6122, 2014.
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(DOI: https://doi.org/10.1109/PATMOS.2013.6662179)

IC.9. D. Zoni and W. Fornaciari, "Sensor-wise methodology to face NBTI stress of NoC buffers", *Design, Automation & Test in Europe Conference & Exhibition (DATE)*, Grenoble, France, 2013, pp. 1038-1043, 2013.
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IC.8. D. Zoni and W. Fornaciari, "NBTI-aware design of NoC buffers", *Interconnection Network Architecture: On-Chip, Multi-Chip (INA-OCMC '13)*, ACM, New York, NY, USA, 25-28, 2013.
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IC.4. D. Zoni, S. Corbetta and W. Fornaciari, "HANDS: heterogeneous architectures and networks-on-chip design and simulation", *ACM/IEEE international symposium on Low power electronics and design (ISLPED '12)*, ACM, New York, NY, USA, 261-266, 2012.
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IC.3. A. Sansottera, D. Zoni, P. Cremonesi and W. Fornaciari, "Consolidation of multi-tier workloads with performance and reliability constraints", *International Conference on High Performance Computing & Simulation (HPCS)*, Madrid, 2012, pp. 74-83, 2012.
(DOI: http://dx.doi.org/10.1109/HPCSim.2012.6266893)

IC.2. C. Brandolese,W. Fornaciari, L. Rucco and D. Zoni, "Towards Energy-Efficient Functional Configuration in WSNs", *11th IFAC,IEEE International Conference on Programmable Devices and Embedded Systems*, Volume 45, Issue 7, 2012, Pages 37-42, 2012.
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IC.1. D. Zoni, P. Bellasi and W. Fornaciari, "A low-overhead heuristic for mixed workload resource partitioning in cluster-based architectures", *25th international conference on Architecture of Computing Systems (ARCS'12)*, Heidelberg, Berlin, 86-97, 2012.
(DOI: http://dx.doi.org/10.1007/978-3-642-28293-5_8)

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IB.1. D. Zoni, P. Englezakis, K. Chrysanthou, A. Canidio, A. Prodromou, A. Panteli, C. Nicopoulos, G. Dimitrakopoulos, Y. Sazeides and W. Fornaciari, "Monitor and Knob Techniques in Network-on-Chip ArchitecturesHarnessing Performance Variability in Embedded and High-performance Many/Multi-core Platforms", Springer, pages 187-213, 2019. (DOI: 10.1007/978-3-319-91962-1_9). Part of ISBN: 9783319919614. Book title: "Harnessing Performance Variability in Embedded and High-performance Many/Multi-core Platforms", W. Fornaciari and D. Soudris editors.

PATENTS

PT.2. D. Zoni and W. Fornaciari, "A computing platform for preventing side channel attacks", N. 102020000013390, POLIMI-DEIB reference number: DEIB.20.026.A, POLIMI-TTO reference number: P06583/IT – AF - 2020 (Title in Italian: "Una piattaforma informatica per prevenire attacchi ai canali laterali"). (PATENT PENDING).

PT.1. D. Zoni and W. Fornaciari, "A computing platform and method for synchronize the prototype execution and simulation of hardware devices ", N. 102020000010531, POLIMI-DEIB reference number: DEIB.20.013.A, POLIMI-TTO reference number: P06554/IT – AF - 2020 (PATENT PENDING).

KEYNOTES

KN.1. "Opportunities and challenges to design an open-hardware SoC in the IoT era", **Keynote** - 27th Euromicro International Conference on Parallel, Distributed and Network-based Processing (PDP), Pavia, italy, Feb, 2019.

TUTORIALS

TT.1. "A hardware-side perspective on the principles and practices to design secure and efficient computing platforms for IoT", **Half-day tutorial** - HiPEAC 2020, Bologna, Italy, Jan, 2020.

INVITED TALKS AND SEMINARS

TK.5. "Analysis and countermeasures to side-channel attacks: a hardware design perspective", **Talk** - 14th International Symposium on Reconfigurable Communication-centric Systems-on-Chip (ReCoSoC 2019), York, UK, July, 2019 .

TK.4. "Towards GPU-aware System Wide Cache Hierarchy for Graphic Workloads", **Talk** - ARM, Cambridge, UK, December, 2015.

TK.3. "Dynamic Voltage Frequency Scaling in Networks-on-Chip: use it without abuse it", **Talk** - University of Cyprus, Nicosia, Cyprus, April, 2015.

TK.2. "Adaptive routing and dynamic frequency scaling for NoC power-performance optimizations", **Talk**, IEEE PATMOS, Karlsrhue, GERMANY, September, 2013.

TK.1. "Consolidation of multi-tier workloads with performance and reliability constraints", **Seminar** to present the Minor Research project, DEIB - Politecnico di Milano, June, 2011.

PHD THESIS

TH.1. D. Zoni, "Exploring power reliability and performance aspects in on-chip networks for multi-cores", Ph.D. in Information Technology at Politecnico di Milano (cum laude) on March 21, 2014. Advisor: Prof. *W. Fornaciari*, Reviewers: Prof. *C. Brandolese*, Prof. *F. Catthoor* (IMEC, Belgium), Prof. *J. Flich* (UPV, Spain), Prof. *D. Soudris* (ICCS,Greece).

TOOLS AND INTELLECTUAL PROPERTIES (IPS): DESIGN AND IMPLEMENTATION

The reported tools and IPs are the result of software and/or hardware projects for which I contributed as principal investigator. Note that the list reported below does NOT contain any tool that has been specifically developed to support only the claim of a single or of a small group of papers. In general, such products are available under Non-Disclosure-Agreement (NDAs) and Non-Commercial Agreements (NCAs) and the majority of them has been partially supported by public and/or private funding. They are actively used by master and PhD students within the HEAPLab[9] research group at Politecnico di Milano to support their research activities and they are also part of my current technology transfer and research activities.

TL.6. **Inspect**
Type - Software tool, Research and Technology Transfer
Description - Automatic and fast pinpointing of the hardware-level components showing a side-channel information leakage in the target computing platform
Kick-off - Jan 2019 (Status - Active)
Principal investigator - D. Zoni, Politecnico di Milano, Italy
Contact - davide.zoni@polimi.it
Funders - 360 Capital Partners[10] via the Poli360 fund (May, 2020 - ongoing)
Contacts - Dr. Paola Bagnoli (paola.bagnoli@polimi.it) - Technology Transfer Office (TTO), Politecnico di Milano

TL.5. **LAMP: Lightweight Application-specific Processor**
Type - IP, Research and Technology Transfer
Description - Production-grade microcontroller-based embedded platform in SystemVerilog targeting Xilinx FPGAs with the goal of supporting the research in the computer architecture research area with particular emphasis on hardware security and machine learning
Kick-off - Jul 2017 (Status - Active)
Principal investigator - D. Zoni, Politecnico di Milano, Italy
Contact - davide.zoni@polimi.it
Funders - 360 Capital Partners [10] via the Poli360 fund (May, 2020 - ongoing)
Contacts - Dr. Paola Bagnoli (paola.bagnoli@polimi.it) - Technology Transfer Office (TTO), Politecnico di Milano
Website - www.lamp-platform.org

TL.4. **GreenHLS**
Type - Software tool, Research and Technology Transfer
Description - Automatic instrumentation of Verilog/Systemverilog descriptions to improve the functionality of a generated digital computing platform. The solution ensures better implementation properties than pure High-Level-Synthesis-based methodologies, while improving the time-to-market with respect to traditional hand-made hardware design methodologies
Kick-off - May 2017 (Status - Active)
Principal investigators - L. Cremona, W. Fornaciari, and D. Zoni (Politecnico di Milano, Italy)
Contact - {luca.cremona,william.fornaciari,davide.zoni}@polimi.it
Funders - Eurolab4HPC[11] via the Business Prototypin Project (BPP) grant (Dec 15, 2019 - April 30, 2020)
Contacts - Vicky Wandels (vicky.wandels@ugent.be) - Ghent University, Belgium
Funders - EU-H2020-MANGO[12] (Oct 1, 2015 - Mar 31, 2019)
Contacts - Jose Flich (jflich@disca.upv.es) - Project coordinator - Universitat Politecnica de Valencia, Valencia, Spain

TL.3. **Multi-precision FPU**
Type - IP, Research and Technology Transfer
Description - Hardware design and implementation of a multi-precision FPU for embedded systems using SystemVerilog. The project includes a companion LLVM compiler pass to further optimize the performance of the executed applications
Kick-off - July 2018 (Status - Completed in 2020)
Principal investigator - D. Zoni, Politecnico di Milano, Italy
Funders - OPRECOMP[13] via the OPRECOMP Summer of Code 2019 grant (Dec 15, 2018 - Sept, 2019)
Contacts - Vicky Wandels (vicky.wandels@ugent.be) - Ghent University, Belgium
Website - https://gitlab.com/davide.zoni/bfloat_fpu_systemverilog

TL.2. **Software to support teaching activities in digital design courses**
Type - Software tool, Teaching activities
Description - Distributed and parallel verification/validation framework for VHDL/Verilog designs using the Xilinx

[9] http://heaplab.deib.polimi.it/
[10] http://www.360cap.vc/
[11] http://www.eurolab4hpc.eu/
[12] https://cordis.europa.eu/project/id/671668
[13] http://www.oprecomp.eu

toolchain. The framework leverages git and ssh to ensure isolation and security. The framework has been used to automatically validate the students' projects of the course "Prova Finale progetto di Reti Logiche"
Kick-off - May 2017 (Status - Completed in 2017)
Principal investigator - D. Zoni, Politecnico di Milano, Italy
Website - https://gitlab.com/davide.zoni/verificatore_prova_finale_reti_logiche_bsc_polimi

TL.1. **HANDS - Heterogeneous Architectures and Networks-on-chip Design and Simulation**
Type - Software tool, Research
Description - cycle-accurate simulation infrastructure to assess power, performance, thermal, and reliability aspects of large multi-cores with novel uncore architectures, i.e., on-chip memory hierarchy and on-chip interconnect
Kick-off - Jul 2012 (Status - Completed in 2016)
Principal investigators - S. Corbetta, W. Fornaciari, and D. Zoni, Politecnico di Milano, Italy
Contact - simone.corbetta@elet.polimi.it, {william.fornaciari,davide.zoni}@polimi.it
Funders - EU-FP7-HARPA[14] (Sep 1, 2013 - Nov 30, 2016)
Contacts - William Fornaciari (william.fornaciari@polimi) - Project coordinator - Politecnico di Milano, Milano, Italy

REFERENCES

All the documents referenced in this curriculum vitae are available upon request.

Milan, March 31, 2022

Signature

Davide Zoni

Autorizzo al trattamento dati ai sensi del GDPR 2016/679 del 27 aprile 2016 (Regolamento Europeo relativo alla protezione delle persone fisiche per quanto riguarda il trattamento dei dati personali). Autorizzo la pubblicazione del Curriculum Vitae sul sito istituzionale del Politecnico di Milano (sez. Amministrazione Trasparente) in ottemperanza al D. Lgs n. 33 del 14 marzo 2013 (e s.m.i.).

[14] https://cordis.europa.eu/project/id/612069